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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,772	01/14/2004	Francesco Pappalardo	854063.740	5496

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EXAMINER	
HOUSHMAND, HOOMAN	

ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,772	PAPPALARDO ET AL.	
	Examiner	Art Unit	
	Hooman Houshmand	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4-7, 9-16, and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Curran (US 5572736).

Regarding **Claim 1**:

Curran teaches:

A method for transmitting data on a bus (col 1 lines 16-18) with minimization of the bus switching activity (col 2 lines 6-8), comprising the steps of: converting the datum (bits) to be transmitted from its own original format into a transmission format (switching codes and code word col 2 lines 5-8, col 4 lines 51-59) that reduces the bus switching activity (minimize the number of bits which switch between the zero and one states col 2 lines 2-14), said step of converting including: swapping the position of one or more bits of the datum to be transmitted (a function of the data word to be transmitted col 2 lines 10-11), said swapping being performable according to a plurality of different variants (The resulting code words represent the possible code words which could be transmitted col 2 lines 32-34), each of which is identified by a respective sorting pattern (A set of maximally distant mappings is derived col 2 lines 30-31, col 2 lines 59-65); and

selecting, between the various sorting patterns (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35), a sorting pattern that reduces the bus switching activity upon transmission on the bus (the number of bus drivers to be switched reduced col 2 lines 36-37) of the datum generated using said selected sorting pattern (switching code identifying the mapping code col 2 lines 60-63); transmitting on the bus the datum in said transmission format; transmitting on the bus the selected sorting pattern (switching code identifying the mapping code col 2 lines 60-65); receiving the datum in said transmission format (receiving circuit); receiving the selected sorting pattern transmitted on the bus (code word); and converting the datum received from said transmission format to said original format using the selected sorting pattern received (receiving circuit, maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65).

Regarding **Claim 4**:

Curran teaches:

A method wherein the sorting pattern selected reduces the bus switching activity (zero and one switching) to a minimum amount (minimize the number of bits which switch between the zero and one states col 2 lines 6-7) and the sorting pattern selected is the optimal (reduced delta-I noise and power consumption) sorting pattern (the number of bit drivers which are required to switch between the zero and one position is reduced, thereby substantially reducing the delta-I noise and power consumption col 2 lines 55-58).

Regarding **Claim 5**:

Curran teaches:

A method, characterized in that each of said steps of generating a succession of sorting patterns (set of maximally distant mappings is derived col 2 lines 30-31) comprises the steps of: providing a finite state machine (a model of the algorithm) having a number of internal states (the generated code words) equal to the number of possible swaps of the position of the bit or bits of the datum to be transmitted (plurality of the generated code words, the one which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55); associating to each of the internal states of said finite state machine a respective sorting pattern (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46); and operating said finite state machine at a given frequency so as to cause its internal state to evolve (compute) and generate said sorting patterns (Each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 6**:

Curran teaches:

A method, characterized in that each of said steps of generating a succession of sorting patterns comprises the step of: generating a plurality of disjoint sets of sorting patterns (set of maximally distant mappings is derived col 2 lines 30-31), each set being formed by a sorting pattern identifying a respective subset of possible swaps of the position of the bit or bits of the datum to be transmitted (one of the generated code words which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55), the sorting patterns of each set being further generated in succession and in a synchronous (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) way with respect to the sorting patterns of the other sets (a plurality of mapping codes are generated col 4 lines 44-46).

Regarding **Claim 7**:

Curran teaches:

A method, characterized in that the step of generating a plurality of separate sets of sorting patterns (set of maximally distant mappings is derived col 2 lines 30-31) comprises, for each said set of sorting patterns, the steps of: providing a finite state machine (a model of the algorithm) having a number of internal states (the generated code words) equal to the number of sorting patterns in the set (one of the generated code words which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55); associating to each of the internal states of said finite state machine a respective sorting pattern (a plurality of mapping

codes are generated, each identified by the state of the switch bits col 4 lines 44-46); and operating said finite state machine at a given frequency so as to cause its internal state to evolve (compute) and generate the corresponding sorting patterns (Each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 9**:

Curran teaches:

A device, characterized in that said first and second sorting pattern generating means each comprise a finite state machine (a model of the algorithm) having a number of internal states (the generated code words) equal to the number of possible swaps of the position of the bit or bits of the datum to be transmitted (one of the generated code words which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55), a respective sorting pattern (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46) being associated to each of the internal states of said finite state machine, said finite state machine being operated at a given frequency so as to cause its internal state to evolve (compute) and generate said sorting patterns (Each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted

code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 10**:

Curran teaches:

A device, characterized in that said first and second sorting pattern generating means each comprise a plurality of sorting pattern modules generating a plurality of disjoint sets of sorting patterns (set of maximally distant mappings is derived col 2 lines 30-31), each set being formed by a sorting pattern identifying a respective subset of all the possible swaps of the position of the bit or bits of the datum to be transmitted (one of the generated code words which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55), the sorting patterns of each set being further generated in succession and in a synchronous (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) way with respect to the sorting patterns of the other sets (a plurality of mapping codes are generated col 4 lines 44-46).

Regarding **Claim 11**:

Curran teaches:

A device, characterized in that each of said sorting pattern (set of maximally distant mappings is derived col 2 lines 30-31) generating modules comprises a finite state machine (a model of the algorithm) having a number of internal states (the generated

code words) equal to the number of sorting patterns of the corresponding set (one of the generated code words which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55), a respective sorting pattern being associated to each of the internal states of said finite state machine (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46), said finite state machine being operated at a given frequency so as to cause its internal state to evolve (compute) and generate said sorting patterns (Each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 12**:

Curran teaches:

A computer product (col 1 line 16) loadable into the memory of a processor associated with a bus, said computer product comprising portions of software code that can implement the method (computer system, data is transmitted as a multi-bit data word between units such as processors and memories, by means of bus driver circuits col 1 lines 16-18) when the computer product is run on a digital processor associated to the bus (col 1 lines 17-18).

Regarding **Claim 13**:

Curran teaches:

A method for transmitting n-bit data on a single line, characterized in that the transmission of a datum comprises the steps of: generating in succession all the possible combinations of n bits (code words col 2 lines 31-35); comparing the n-bit datum to be transmitted with the combinations of n bits generated (set of maximally distant mappings derived col 2 lines 30-31); generating and transmitting on a single line an identity signal (minimally distant) upon detection of the coincidence between the n-bit datum to be transmitted and one of the combinations of n bits generated (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35) , and in that the reception of the datum transmitted comprises the steps of: generating a succession of combinations of n bits (mappings) identical to the one generated in transmission (receiver applies reverse mapping to recover the original data word col 4 lines 57-59) and synchronous (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) with respect to the latter; and identifying the combination of n bits generated at the instant of reception of the identity signal transmitted on the single line (At the receiving end, the bits of the code word identified by the switching code are modified to reconstruct the transmitted data word col 3 lines 7-9), the combination of n bits identified being identical to the n-bit datum to be transmitted (receiving circuit maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65).

Regarding **Claim 14**:

Curran teaches:

A method, characterized in that said steps of generating in succession all the possible combinations of n bits (set of maximally distant mappings is derived col 2 lines 30-31) comprises the steps of: providing a finite state machine (a model of the algorithm) having a number of internal states (the generated code words) equal to the number of possible combinations of n bits (plurality of the generated code words, the one which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55); associating to each of the internal states of said finite state machine a respective combination of n bits (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46); and operating said finite state machine at a given frequency so as to cause its internal state to evolve (compute) and generate the corresponding combinations of n bits (Each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 15**:

Curran teaches:

A method, characterized in that said steps of generating the combinations of n bits comprises the steps of: generating a plurality of disjoint sets of possible combinations of

n bits (set of maximally distant mappings is derived col 2 lines 30-32), the combinations of n bits of each set being further generated in succession and in a synchronous (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) way with respect to the combinations of n bits of the other sets (a plurality of mapping codes are generated col 4 lines 44-46).

Regarding **Claim 16**:

Curran teaches:

A method, characterized in that the step of generating a plurality of disjoint sets of possible combinations of n bits (set of maximally distant mappings is derived col 2 lines 30-32) comprises, for each said set of combinations of n bits, the steps of: providing a finite state machine (a model of the algorithm) having a number of internal states (the generated code words) equal to the number of combinations of n bits in the set (plurality of the generated code words, the one which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55); associating to each of the internal states of said finite state machine a respective combination of n bits (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46); and operating said finite state machine at a given frequency so as to cause its internal state to evolve (compute) and generate the corresponding combinations of n bits (Each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The

code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 18**:

Curran teaches:

A device, characterized in that each of said first and second combination generating means comprises a finite state machine (a model of the algorithm) having a number of internal states (the generated code words) equal to the number of possible combinations of n bits (plurality of the generated code words, the one which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55), a respective combination of n bits being associated to each of the internal states of said finite state machine (a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46) , and said finite state machine being operated at a given frequency so as to cause its internal state to evolve (compute) and generate the corresponding combinations of n bits (Each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 19**:

Curran teaches:

A device, characterized in that said first and second combination generating means each comprise a plurality of combination generating modules generating a plurality of disjoint sets of possible combinations of n bits (set of maximally distant mappings is derived col 2 lines 30-32), the combinations of n bits of each set being generated in succession and in a synchronous (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-44) way with respect to the combinations of n bits of the other sets (a plurality of mapping codes are generated col 4 lines 44-46).

Regarding **Claim 20**:

Curran teaches:

A device, characterized in that each of said combination generating modules (set of maximally distant mappings is derived col 2 lines 30-31) comprises a finite state machine (a model of the algorithm) having a number of internal states (the generated code words) equal to the number of combinations of n bits in the set (plurality of the generated code words, the one which differs in the smallest number of bit positions from the previously transmitted code word is selected col 2 lines 51-55), a respective combination of n bits being associated to each of the internal states of said finite state machine(a plurality of mapping codes are generated, each identified by the state of the switch bits col 4 lines 44-46) , and said finite state machine being operated at a given frequency so as to cause its internal state to evolve (compute) and generate the corresponding combinations of n bits (Each of the code words is compared with a

previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle col 4 lines 51-57).

Regarding **Claim 21**:

Curran teaches:

A computer product (col 1 line 16) loadable into the memory of a processor associated with a bus, said computer product comprising portions of software code that can implement the method (computer system, data is transmitted as a multi-bit data word between units such as processors and memories, by means of bus driver circuits col 1 lines 16-18) when the computer product is run on a digital processor associated to the bus (col 1 lines 17-18).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 2, 3, 8, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Curran (US 5572736) in view of Szepesi (US 5680300).

Regarding **Claim 2**:

Curran teaches:

A method wherein said step of transmitting on the bus the selected sorting pattern comprises the steps of: generating a succession of sorting patterns identifying all the possible swaps of the position of the bit or bits of the datum to be transmitted (resulting code words represent the possible code words which could be transmitted col 2 lines 32-34); comparing the optimal sorting pattern to be transmitted with the sorting patterns generated (set of maximally distant mappings derived col 2 lines 30-31); generating and transmitting on the bus a synchronization (push-pull bus driver col 4 lines 6-21) signal upon detection of the identity (minimally distant) between the optimal sorting pattern to be transmitted and one of the sorting patterns generated (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35).

Curran does not teach: push-pull bus driver used for synchronization.

Szepesi teaches: synchronization with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field; using electronics for timing, their art is analogous.

Teachings of Szepesi and Curran can be combined - using a push-pull drive to achieve synchronization - to produce the applicant's invention.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Regarding **Claim 3**:

Curran teaches:

A method wherein said step of receiving the selected sorting pattern transmitted on the bus comprises the steps of: generating a succession of sorting patterns (mappings) identical to, and synchronous (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) with, the one generated in transmission (receiver applies reverse mapping to recover the original data word col 4 lines 57-59); and identifying the sorting pattern generated at the instant of reception of the synchronization (push-pull bus driver col 4 lines 6-21) signal transmitted on the bus (At the receiving end, the bits of the code word identified by the switching code are modified to reconstruct the transmitted data word col 3 lines 7-9), the sorting pattern identified

being identical to said selected sorting pattern to be transmitted (receiving circuit maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65).

Curran does not teach: push-pull bus driver used for synchronization.

Szepesi teaches: synchronization with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field; using electronics for timing, their art is analogous.

Teachings of Szepesi and Curran can be combined - using a push-pull drive to achieve synchronization - to produce the applicant's invention.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Regarding **Claim 8**:

Curran teaches:

A device for transmitting data on a bus (col 1 lines 16-18) with minimization of the bus switching activity (col 2 lines 6-8), comprising: first converting means for converting the

datum (bits) to be transmitted from its own original format to a transmission format (switching codes and code word col 2 lines 5-8, col 4 lines 51-59) that minimizes the bus switching activity (minimize the number of bits which switch between the zero and one states col 2 lines 2-14), said first converter means comprising: a swap operator for swapping the position of one or more bits of the datum to be transmitted (a function of the data word to be transmitted col 2 lines 10-11), said swapping being performable according to a plurality of different variants (The resulting code words represent the possible code words which could be transmitted col 2 lines 32-34), each of which is identified by a respective sorting pattern (A set of maximally distant mappings is derived col 2 lines 30-31); and selecting means for selecting, between the various sorting patterns (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35), an optimal sorting pattern that minimizes the bus switching activity (the number of bus drivers to be switched reduced col 2 lines 36-37) upon transmission on the bus of the datum generated using said optimal sorting pattern (switching code identifying the mapping code col 2 lines 60-63); said transmission device further comprising: transmitting means for transmitting on the bus the datum in said transmission format and the optimal sorting pattern; receiving means for receiving the datum in said transmission format and said optimal sorting pattern (code word) transmitted on the bus; and second converting means for converting the datum received from said transmission format to said original format using said optimal sorting pattern received (receiving circuit, maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65),

said transmission device being characterized in that said transmitting means comprise: first sorting pattern generating means for generating a succession of sorting patterns identifying all the possible swaps of the position of the bit or bits of the datum to be transmitted (resulting code words represent the possible code words which could be transmitted col 2 lines 32-34); comparing means for comparing the optimal sorting pattern to be transmitted with the sorting patterns generated (set of maximally distant mappings derived col 2 lines 30-31); signal generating means for generating and sending onto said bus a synchronization (push-pull bus driver col 4 lines 6-21) signal upon detection of the identity (minimally distant) between the optimal sorting pattern to be transmitted and one of the sorting patterns generated (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35),
said transmission device being further characterized in that said receiving means comprise: second sorting pattern generating means for generating a succession of sorting patterns (mappings) identical to, and synchronous (instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) with, the one generated in transmission (receiver applies reverse mapping to recover the original data word col 4 lines 57-59); and detecting means for identifying the sorting pattern generated at the instant of reception of the synchronization (push-pull bus driver col 4 lines 6-21) signal transmitted on the bus (At the receiving end, the bits of the code word identified by the switching code are modified to reconstruct the transmitted data word col 3 lines 7-9), the sorting pattern identified being identical to said optimal sorting

pattern to be transmitted (receiving circuit maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65).

Curran does not teach: push-pull bus driver used for synchronization.

Szepesi teaches: synchronization with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field; using electronics for timing, their art is analogous.

Teachings of Szepesi and Curran can be combined - using a push-pull drive to achieve synchronization - to produce the applicant's invention.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Regarding **Claim 17**:

Curran teaches:

A device for transmitting n-bit data on a single line, characterized in that it comprises, at the transmission end: first combination generating means for generating in succession all the possible combinations of n bits (resulting code words represent the possible code

words which could be transmitted col 2 lines 32-34); comparing means for comparing the n-bit datum to be transmitted with the combinations of n bits generated (set of maximally distant mappings derived col 2 lines 30-32); signal generating means for generating and transmitting on a single line an identity signal upon detection (minimally distant) of the coincidence between the n-bit datum to be transmitted and one of the combinations of n bits generated (the code word which is minimally distant from the previous code word is selected col 2 lines 34-35); and in that it comprises, at the reception end: second combination generating means for generating the same succession of combinations of n bits (receiver applies reverse mapping to recover the original data word col 4 lines 57-59), generated by the first combination generating means, the successions of combinations of n bits generated by the said first and second combination-generating means being synchronized (push-pull bus driver col 4 lines 6-21; instead of complementing an entire word - bus inverted – mapping codes are generated col 4 lines 42-59) with one another; and detecting means for identifying the combination of n bits generated at the instant of reception of the identity signal transmitted on the single line (At the receiving end, the bits of the code word identified by the switching code are modified to reconstruct the transmitted data word col 3 lines 7-9) , the combination of n bits identified being identical to the n-bit datum to be transmitted (receiving circuit maps the received code word into the original data word, as that data word existed prior to transmission col 2 lines 63-65).

Curran does not teach: push-pull bus driver used for synchronization.

Szepesi teaches: synchronization with push-pull drive (col 6 lines 18-34).

Both Szepesi and Curran are in the electronics field; using electronics for timing, their art is analogous.

Teachings of Szepesi and Curran can be combined - using a push-pull drive to achieve synchronization - to produce the applicant's invention.

It would have been obvious; at the time the invention was made, for a person having ordinary skill in the art to combine the teachings of Szepesi with Curran to produce accurate reception of data at the receiver.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hooman Houshmand whose telephone number is 571-270-1817. The examiner can normally be reached on Monday - Friday 8 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HH

CHARLES D. GARBER
SUPERVISORY PATENT EXAMINER